In the Claims:

Claim 1 (currently amended): A method of fabricating a semiconductor device, having a nitride/high-k material/nitride gate dielectric stack, comprising:

initiating formation of the nitride/high-k material/nitride gate dielectric stack by:

depositing a first ultra-thin nitride film on a semiconductor substrate, wherein the first ultra-thin nitride film is deposited by using an atomic layer deposition (ALD) technique;

depositing a high-k material on the first ultra-thin nitride film, wherein the high-k material comprises a thin metal film, and wherein the thin metal film comprises at least one material selected from a group consisting essentially of zirconium (Zr), hafnium (Hf), and titanium (Ti); and

depositing a second ultra-thin nitride film on the high-k material, thereby forming a sandwich structure, wherein the second ultra-thin nitride film is deposited using an atomic layer deposition (ALD) technique;

depositing a ~~thick~~ gate material on the second ultra-thin nitride film, wherein said gate material comprises polysilicon-germanium (poly-SiGe);

completing formation of the nitride/high-k material/nitride gate dielectric stack from the sandwich structure; and

completing fabrication of the device;

wherein the first and second ultra-thin nitride films prevent the at least one material selected from the group consisting essentially of zirconium (Zr), hafnium (Hf), and titanium (Ti) from diffusing into the semiconductor substrate and the ~~thick~~ gate material, respectively.

Claim 2 (previously presented): A method as recited in claim 1, wherein the substrate comprises a silicon-on-insulator (SOI) wafer.

Claim 3 (previously presented): A method as recited in claim 1, wherein the first ultra-thin nitride film comprises silicon nitride (Si_3N_4), and wherein the first ultra-thin nitride film has a thickness in a range of 1 to 2 atomic layer(s).

Claim 4 (canceled).

Claim 5 (previously presented): A method as recited in claim 1, wherein the thin metal film further comprises tantalum (Ta).

Claim 6 (original): A method as recited in claim 1, wherein the thin metal film comprises a metal oxide.

Claim 7 (previously presented): A method as recited in claim 1, wherein the

second ultra-thin nitride film comprises silicon nitride (Si_3N_4), and wherein the second ultra-thin nitride film has a thickness in a range of 1 to 2 atomic layer(s).

Claim 8 (currently amended): A method as recited in claim 1, wherein completing formation of the nitride/high-k material/nitride gate dielectric stack from the sandwich structure comprises:

patterning the ~~thick~~ gate material, thereby forming a gate electrode; and

etching portions of the sandwich structure uncovered by the gate electrode, thereby completing formation of the nitride/high-k material/nitride gate dielectric stack.

Claim 9 (original): A method as recited in claim 1, wherein completing fabrication of the device comprises forming of a MOSFET structure comprising the gate dielectric stack.

Claim 10 (currently amended): A method as recited in claim 8, ~~wherein the thick gate material comprises a material selected from a group consisting essentially of polysilicon (poly-Si) and polysilicon-germanium (poly-SiGe), and~~ wherein the ~~thick~~ gate material is patterned using a material such as photoresist.

Claim 11 (original): A method as recited in claim 1, wherein completing fabrication of the device comprises:

forming a source/drain structure in the substrate and flanking the gate dielectric stack;

forming at least one spacer on at least one sidewall of the gate dielectric stack; and

silicidizing a shallow source/drain region as well as the high-k gate stack, thereby forming a source/drain silicide in a shallow source/drain region of the substrate and a gate silicide on the gate dielectric stack.

Claim 12 (currently amended): A method of fabricating a semiconductor device, having a nitride/high-k material/nitride gate dielectric stack, comprising:

initiating formation of the nitride/high-k material/nitride gate dielectric stack by:

depositing a first ultra-thin nitride film on a semiconductor substrate, wherein the first ultra-thin nitride film is deposited by using an atomic layer deposition (ALD) technique, and wherein the substrate comprises a silicon-on-insulator (SOI) wafer;

depositing a high-k material on the first ultra-thin nitride film, wherein the high-k material comprises a thin metal film, and wherein the thin metal film comprises at least one material selected from a group consisting essentially of zirconium (Zr), hafnium (Hf), and titanium (Ti); and

depositing a second ultra-thin nitride film on the high-k material, thereby forming a sandwich structure, wherein the second ultra-thin nitride film is deposited by using an atomic layer deposition (ALD) technique;

depositing a ~~thick~~ gate material on the second ultra-thin nitride film, wherein said gate material comprises polysilicon-germanium (poly-SiGe);

completing formation of the nitride/high-k material/nitride gate dielectric stack from the sandwich structure; and

completing fabrication of the device;

wherein the first and second ultra-thin nitride films prevent the at least one material selected from the group consisting essentially of zirconium (Zr), hafnium (Hf), and titanium (Ti) from diffusing into the semiconductor substrate and the ~~thick~~ gate material, respectively.

Claim 13 (previously presented): A method as recited in claim 12, wherein the first ultra-thin nitride film comprises silicon nitride (Si_3N_4), and wherein the first ultra-thin nitride film has a thickness in a range of 1 to 2 atomic layer(s).

Claim 14 (previously presented): A method as recited in claim 13, wherein the thin metal film further comprises tantalum (Ta), and wherein the thin metal film further comprises a metal oxide.

Claim 15 (previously presented): A method as recited in claim 14, wherein the second ultra-thin nitride film comprises silicon nitride (Si_3N_4), and wherein the second ultra-thin nitride film has a thickness in a range of 1 to 2 atomic layer(s).

Claim 16 (currently amended): A method as recited in claim 15, wherein completing formation of the nitride/high-k material/nitride gate dielectric stack from the sandwich structure comprises:

patterning the ~~thick~~ gate material, thereby forming a gate electrode; and

etching portions of the sandwich structure uncovered by the gate electrode, thereby completing formation of the nitride/high-k material/nitride gate dielectric stack.

Claim 17 (original): A method as recited in claim 16, wherein completing fabrication of the device comprises forming of a MOSFET structure comprising the gate dielectric stack.

Claim 18 (currently amended): A method as recited in claim 17, ~~wherein the thick gate material comprises a material selected from a group consisting essentially of polysilicon (poly-Si) and polysilicon-germanium (poly-SiGe), and~~ wherein the ~~thick~~ gate material is patterned using a material such as photoresist.

Claim 19 (original): A method as recited in claim 18, wherein completing fabrication of the device comprises:

forming a source/drain structure in the substrate and flanking the gate dielectric stack;

forming at least one spacer on at least one sidewall of the gate dielectric stack; and

silicidizing a shallow source/drain region as well as the high-k gate stack, thereby forming a source/drain silicide in a shallow source/drain region of the substrate and a gate silicide on the gate dielectric stack.

Claim 20 (canceled).